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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/264,501	03/08/1999	ROGER PANICACCI	08305/026001	3217

20985 7590 01/02/2003

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EXAMINER
WU, DOROTHY

ART UNIT	PAPER NUMBER
2697	

DATE MAILED: 01/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/264,501	PANICACCI ET AL.	
	Examiner	Art Unit	
	Dorothy Wu	2697	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-13,17-23,26,27,31-37* is/are rejected.

7)☒ Claim(s) *11,14,15,16,24,25,28,29,30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

NOT DONE

1. New corrected drawings are required in this application because the drawings have been objected to under 37 CFR 1.84 or 1.152 for the reasons indicated on the Notice of Draftsperson's Patent Drawing Review. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

✓ 2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "49A" and "49B" in Fig. 4. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: On page ✓ 12, lines 9-10, the analog multiplexer is disclosed without a reference character. On page ✓ 20, lines 7-8, the disclosure cites a binary-scaled network of capacitors "C11, C12, C18," whereas interpretation of the corresponding drawing reveals that the network comprises capacitors C11 through C18. Subsequent citations of the capacitors of the binary-scaled network should be similarly noted. On

page 25, lines 19-20, the disclosure cites a calibration network which includes a network of capacitors "C19, C24, C25, C26," whereas interpretation of the corresponding drawing reveals that the network comprises capacitors C19 through C24, C25, and C26. Subsequent citations of the capacitors of the calibration network should be similarly noted. Appropriate correction is required.

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 12, the parent claim of claim 13, claims a calibration network. Claim 13 cites claim 12 as its parent claim, "further including: a second binary-scaled capacitor network." Interpretation of the specification reveals that the second binary-scaled capacitor network is the calibration network. However, because of the phrase "further including," the circuit of claim 13 includes both a calibration network and a separate second binary-scaled capacitor network. The same objection is applied to claim 27 in relation to parent claim 26.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 19-30 are rejected under 35 U.S.C. 112, second paragraph.

Claims 19-30 recite the limitation "readout circuit." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Vu et al, U.S. Patent 6,025,875.

Regarding claim 6, Vu teaches a circuit that reads out values from an active pixel sensor array (col. 3, lines 65-67). Vu teaches a correlated double sampling circuit that samples and holds an input signal reference and a pixel value, and calculates the difference between the two signals (col. 7, lines 33-37, and Fig. 7). Vu also teaches an operational amplifier-based charge sensing circuit that provides an amplified differential output signal based on signals provided by the correlated double sampling circuit (col. 7, lines 1 – 32, 39-42, and Fig. 6). Because the read-out circuit handles one video signal, it is an inherent property of the circuit to be associated with a single column in the sensor array.

Regarding claim 7, Vu teaches an array of capacitors that can be selectively enabled to choose a gain associated with the operational amplifier based charge sensing circuit (col. 5, lines 49-53, Fig. 6, and Fig. 9).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being anticipated by Vu et al, U.S. Patent 6,025,875, in view of Wong, U.S. Patent 5,708,263.

Regarding claim 1, Vu teaches a circuit that reads out values from a contact image sensor, an active pixel sensor array (col. 3, lines 65-67). Vu teaches a correlated double sampling circuit that samples and holds an input signal reference and a pixel value, and calculates the difference between the two signals (col. 7, lines 33-37, and Fig. 7). Vu also teaches an operational amplifier-based charge sensing circuit that provides an amplified differential output signal based on signals provided by the correlated double sampling circuit (col. 7, lines 1 – 32, 39-42, and Fig. 6). Vu does not teach two separate sample-and-hold circuits for sampling and storing signals from pixels in a first and second column, nor does he teach that the operational amplifier-based charge sensing circuit is associated with only the first and second columns. Wong teaches the method of multiplexing between columns to selectively enable one of two columns to be read out at a time (col. 5, lines 26-37, and Fig. 1B).

Therefore, it would have been obvious to one of ordinary skill at the time the invention was made to combine the correlated double sampling and operational amplifier-based charge sensing circuits taught by Vu with the practice of multiplexing columns taught by Wong to make a read-out circuit comprising two correlated double sampling circuits associated with a first and

second column and an operational amplifier-based charge sensing circuit associated only with the first and second columns that produced an amplified differential output based on signals from the first or second correlated double sampling circuit. One of ordinary skill would be motivated to make such a modification because the practice of multiplexing columns reduces the amount of needed hardware and creates a read-out circuit of smaller area.

Regarding claim 2, Vu teaches an array of capacitors that can be selectively enabled to choose a gain associated with the operational amplifier based charge sensing circuit (col. 5, lines 49-53, Fig. 6, and Fig. 9).

Regarding claim 3, Wong teaches the method of multiplexing between columns to selectively enable one of two columns to be read out at a time (col. 5, lines 26-37, and Fig. 1B). Vu teaches an array of capacitors that can be selectively enabled to choose a gain associated with the operational amplifier-based charge sensing circuit (col. 5, lines 49-53, Fig. 6, and Fig. 9).

Regarding claim 4, Vu teaches a clamping circuit that selectively adds a pre-gain offset voltage to a signal about to be sampled (col. 4, lines 6-27, and Fig. 5).

Regarding claim 5, Vu teaches a switched capacitor integrator in the operational amplifier-based charge sensing circuit (Fig. 6)

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vu et al, U.S. Patent 6,025,875, in view of Susak, U.S. Patent 6,118,400. Vu teaches a circuit that reads out values from an active pixel sensor array (col. 3, lines 65-67). Vu teaches a correlated double sampling circuit that samples and holds an input signal reference and a pixel value, and calculates the difference between the two signals (col. 7, lines 33-37, and Fig. 7). Vu also teaches

an operational amplifier-based charge sensing circuit that provides an amplified differential output signal based on signals provided by the correlated double sampling circuit (col. 7, lines 1 – 32, 39-42, and Fig. 6). Because the read-out circuit handles one video signal, it is an inherent property of the circuit to be associated with a single column in the sensor array. Vu does not teach an analog-to-digital converter for converting an input to a corresponding digital output using a successive approximation technique. Susak teaches an analog-to-digital converter for converting an input to a corresponding digital output using a successive approximation technique (col. 1, lines 23-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add an analog-to-digital converter for converting an input to a corresponding digital output using a successive approximation technique to the circuit taught by Vu. One of ordinary skill would be motivated to make such a modification because it is common in the art of image processing to convert an analog signal to a digital signal for the purpose of executing digital signal processing to improve the quality of the signal.

9. Claims 8-10, 18-23, and 31-34 are rejected under 35 U.S.C. 103(a) as being anticipated by Vu et al, U.S. Patent 6,025,875, in view of Wong, U.S. Patent 5,708,263, and further in view of Susak, U.S. Patent 6,118,400.

Regarding claim 8, Vu in view of Wong teach a circuit for reading out pixels from an active pixel sensor array comprising first and second sample-and-hold circuits for sampling and storing signals from pixels in a first and second column, and an operational amplifier based charge sensing circuit, associated with only the first and second columns, that selectively

provides an amplified differential output signal based on signals sampled by either the first or second sample-and-hold circuit. See above. Vu in view of Wong do not teach an analog-to-digital converter, associated only with the first and second columns, for converting the differential output to a corresponding digital signal using a successive approximation technique. Susak does teach an analog-to-digital converter for converting an input to a corresponding digital output using a successive approximation technique (col. 1, lines 23-26). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add an analog-to-digital converter for converting an input to a corresponding digital output using a successive approximation technique to the circuit taught by Vu in view of Wong. One of ordinary skill would be motivated to make such a modification because it is common in the art of image processing to convert an analog signal to a digital signal for the purpose of executing digital signal processing to improve the quality of the signal.

Regarding claim 31, official notice taken. It is common practice in the art of image sensing technology for active pixel sensors to include rows and columns of sensors, and to select a row of sensors whose values will be read out. Because the apparatus is taught, the method associated with the apparatus is also taught.

Regarding claims 32-34, because the apparatus is taught, the method associated with the apparatus is also taught.

Regarding claim 9, Vu teaches that the operational amplifier-based charge sensing circuit includes a switched capacitor integrator (Fig. 6).

Regarding claim 10, Susak teaches that the analog-to-digital converter includes a first binary-scaled capacitor network (col. 1, lines 35-40). The analog-to-digital converter also

includes a comparator, wherein the capacitors in the first network share a common node coupled to the first input of the comparator, and the analog input signal is coupled to a second input of the comparator (col. 2, lines 56-60, and Fig. 1).

Regarding claim 18, Vu teaches a contact image sensor (col. 3, lines 65-67), well known in the art to be constructed using a CMOS process. Wong teaches an array of active pixel sensors, wherein each sensor is associated with a column (col. 2, lines 40-53). Wong also teaches the method of multiplexing between columns to selectively enable one of two columns to be read out at a time (col. 5, lines 26-37, and Fig. 1B). Regarding the other limitations of the claim, see claim 1, above.

Regarding claim 19, Vu teaches an array of capacitors that can be selectively enabled to choose a gain associated with the operational amplifier based charge sensing circuit (col. 5, lines 49-53, Fig. 6, and Fig. 9).

Regarding claim 20, Wong teaches the method of multiplexing between columns to selectively enable one of two columns to be read out at a time (col. 5, lines 26-37, and Fig. 1B). Vu teaches an array of capacitors that can be selectively enabled to choose a gain associated with the operational amplifier-based charge sensing circuit (col. 5, lines 49-53, Fig. 6, and Fig. 9). Therefore, one of ordinary skill could provide an array of capacitors for each column that can be selectively enabled to choose a gain associated with the operational amplifier-based charge sensing circuit.

Regarding claim 21, Vu teaches a clamping circuit that selectively adds a pre-gain offset voltage to a signal about to be sampled (col. 4, lines 6-27, and Fig. 5).

Regarding claim 22, Vu teaches a switched capacitor integrator in the operational amplifier-based charge sensing circuit (Fig. 6)

Regarding claim 23, Susak teaches that the analog-to-digital converter includes a first binary-scaled capacitor network (col. 1, lines 35-40). The analog-to-digital converter also includes a comparator, wherein the capacitors in the first network share a common node coupled to the first input of the comparator, and the analog input signal is coupled to a second input of the comparator (col. 2, lines 56-60, and Fig. 1).

10. Claims 12, 13, 26, 27, 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vu et al, U.S. Patent 6,025,875, in view of Wong, U.S. Patent 5,708,263, in view of Susak, U.S. Patent 6,118,400, and further in view of Tan, U.S. Patent 4,399,426.

Regarding claim 12, Vu in view of Wong in view of Susak teach the apparatus according to claim 10. See above. Vu in view of Wong in view of Susak do not teach a calibration network for providing a signal to cancel an offset of the comparator. Tan does teach a calibration network to measure, and thus cancel, an offset of the comparator (col. 1, lines 6-7, and col. 10, lines 46-52). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the calibration network taught by Tan to calibrate and cancel the offset of the comparator in the apparatus taught by Vu in view of Wong in view of Susak. One of ordinary skill in the art would be motivated to make such a modification to correct for non-linear errors in the comparator and thus achieve a more accurate signal.

Regarding claims 35 and 37, because the apparatus is taught, the method associated with the apparatus is also taught.

Regarding claim 13, Tan teaches a second binary-scaled capacitor network used to successively approximate and store an error (col. 3, lines 41-44), wherein the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network (Fig.4). Tan teaches that the method can be used to determine the offset of the comparator (col. 10, lines 46-52).

Regarding claim 26, Tan teaches a calibration network to measure, and thus cancel, an offset of the comparator (col. 1, lines 6-7, and col. 10, lines 46-52).

Regarding claim 27, Tan teaches a second binary-scaled capacitor network used to successively approximate and store an error (col. 3, lines 41-44), wherein the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network (Fig.4). Tan teaches that the method can be used to determine the offset of the comparator (col. 10, lines 46-52).

Regarding claim 36, because the apparatus is taught, the method associated with the apparatus is also taught.

Allowable Subject Matter

11. Claims 11, 14, 15, 16, 24, 25, 28, 29, 30 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dorothy Wu whose telephone number is 703-305-8412. The examiner can normally be reached on Monday-Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Williams can be reached at 703-305-4863.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC 20231

Or faxed to:

703-872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is 703-306-0377.

KA Williams

Kimberly A. Williams
Primary Examiner
~~Technology Center 2700~~

Dorothy Wu

DW
December 23, 2002